Readiness and requirements of EUVL mask blank in each hp node

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Outline

- Introduction
- Blank defects
  - Printability and inspectability studies in each node
  - Defect reduction roadmap
  - Additional defect mitigation processes
- Pattern defects
  - Printability evaluations in each node
- Non-flatness issues
- Summary & Conclusions

EUV focus areas in 2006-2010

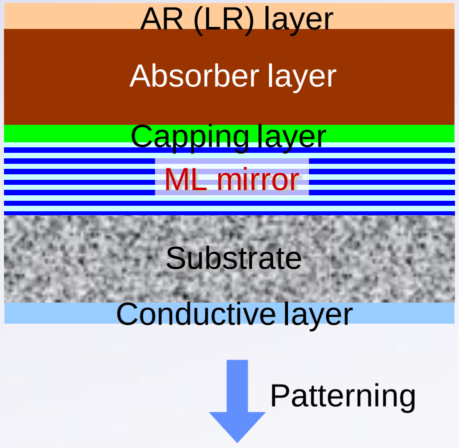
2006 / 32hp	2007 / 22hp	2008 / 22hp	2009 / 22hp	2010 / 22hp
1. Reliable high power source & collector module	1. Reliable high power source & collector module	1. Long-term source operation with 100 W at IF and 5MJ/day	1. Mask yield & defect inspection/review infrastructure	1. Mask yield & defect inspection/review infrastructure
2. Resist resolution, sensitivity & LER met simultaneously	2. Resist resolution, sensitivity & LER met simultaneously	2. Defect free masks through lifecycle & inspection/review infrastructure	2. Long-term reliable source operation with 200 W at IF	1. Long-term reliable source operation with 200 W at IF
3. Availability of defect free mask	3. Availability of defect free mask	3. Resist resolution, sensitivity & LER met simultaneously	3. Resist resolution, sensitivity & LER met simultaneously	2. Resist resolution, sensitivity & LER met simultaneously
4. Reticle protection during storage, handling and use	4. Reticle protection during storage, handling and use	• Reticle protection during storage, handling and use	• EUVL manufacturing integration	• EUVL manufacturing integration
5. Projection and illuminator optics quality & lifetime	5. Projection and illuminator optics quality & lifetime	• Projection / illuminator optics and mask lifetime		

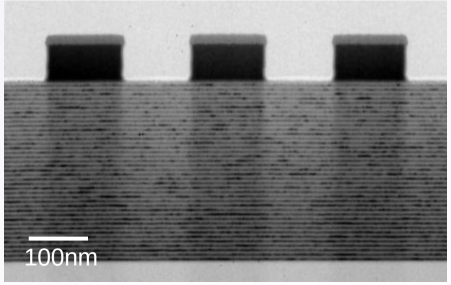
**International EUVL Symposium Program Steering Committee, 2006 - 2010*

- **Mask defects with readiness in related infrastructure are still top concern for successful implementation of EUVL in industry**
  - Among the mask defects, blank defect is more printable and also not easy to be inspected & repaired.
  - Roadmap for defect inspection & review tool is behind the needs from industry.

EUVL mask blank: stacks & materials

Mask blank





Layer	Materials	Main focus	Target
AR (LR)	TaON, TaO, TaBO, etc.	Max contrast @DUV, inspection sensitivity	Sufficient sensitivity for printable defects @ inspector
Absorber	TaN, TaBN, etc.	Litho performances @EUV (contrast, NILS, H-V bias, LWR, OD…)	R_{avg} < 0.2 % (13.465-13.535 nm)
Capping	Ru, Si, etc.	Protecting ML (etch, CLN, repair, C contamination, exposure damage)	Robustness @ various process environments
ML mirror	Mo/Si 40-50 pairs	High reflectivity @EUV	$R_{max} \geq 65$ %
		Low defectivity	Zero printed defects
Substrate	LTEM 6025	Low thermal expansion	< 5 ppb/°C
		Non-flatness	< 35 nm P-V
Backside	CrN	Electrostatic chucking @ EUV scanner	< 100 Ω/□

- **Blank structure should be evolved with decreasing design rule to maximize**
  – Lithography performances in each scanner scheme (NA, CRA, sigma, wavelength, …)
  – Mask inspection performances (257nm, 193nm, actinic, e-beam, …)
  – Mask process extendibility, etc.

Challenge in EUV mask blank

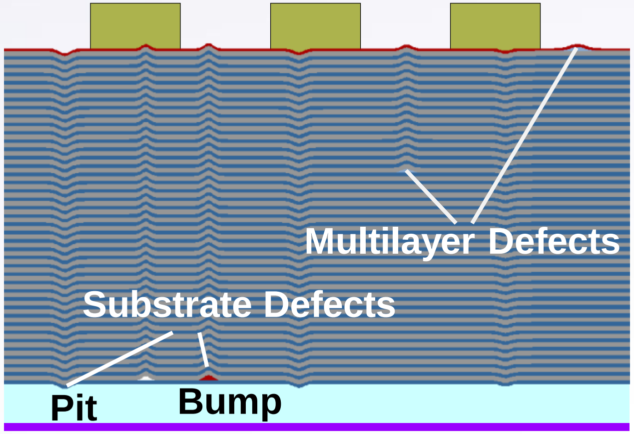
Availability of Defect-Free EUVL Mask

Achieving zero defect for EUVL masks in the next few years is extremely challenging.

Blank's Defect Level required for HVM
< 0.003/cm^2 @25nm

Large Gap

Current Status (2011 2Q champion)
~ 0.5/cm^2 @25nm (estimation)



Defect free blank
- Collaborate with suppliers

Blank inspection
- DUV inspection
- Actinic blank inspection
- Actinic defect review

Pattern inspection
- DUV inspection
- Actinic pattern inspection
- Actinic defect review

Not ready for HVM until ~2015/2016

Tentative solutions
- *Practical defect spec*
- *Wafer inspection*
- *Defect compensation*
- *Phase defect repair*

Industry-wide collaboration is required.

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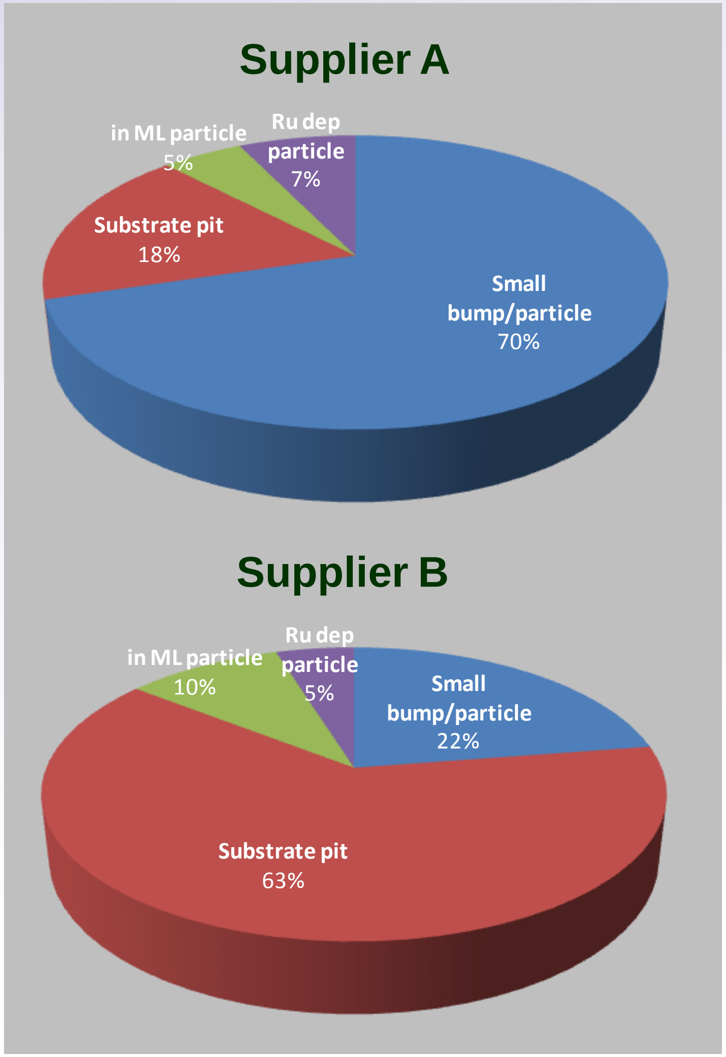
Defect types in commercial blanks



Defect types	Reduction approaches
Small bump/particle	Substrate polishing/cleaning, Mechanical work in IBD
Substrate pit	Substrate polishing, Smoothing during ML deposition
In ML particle	IBD process (shield, target, ion source, etc.)
Ru deposition particle (on ML surface)	Ru deposition (shield, target, etc.), Handling

- Two blank suppliers show different trends in defect type distributions, but majority of defects are originated from substrate. → Substrate polishing/cleaning improvements are required.
- Portions of ML and Ru dep. particles are relatively low, but they are larger than defects from substrate. → They should be tightly controlled.

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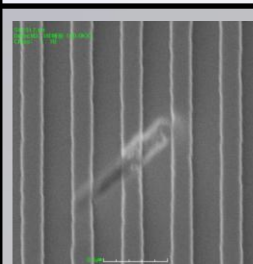
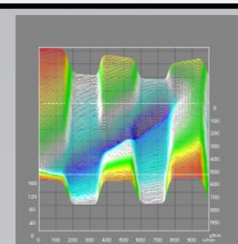
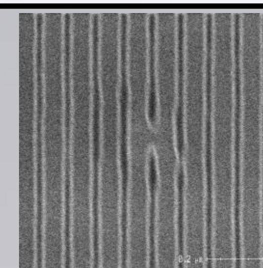
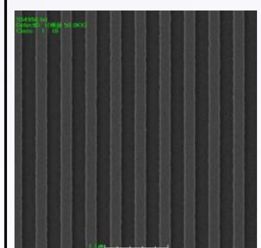
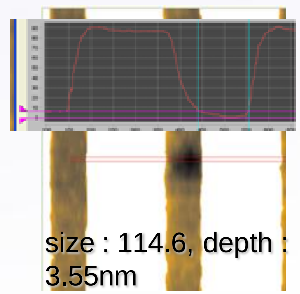
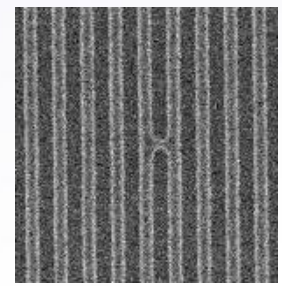
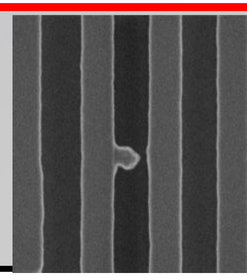
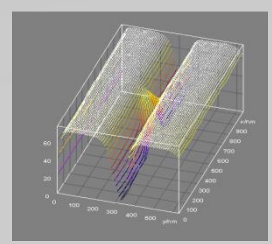
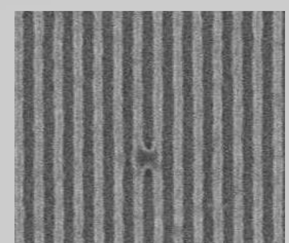
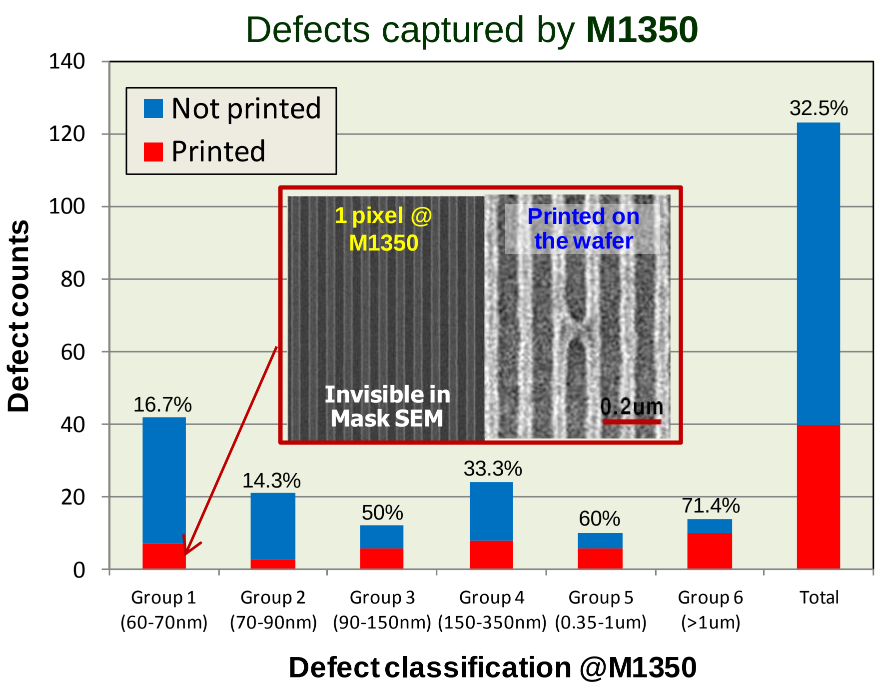
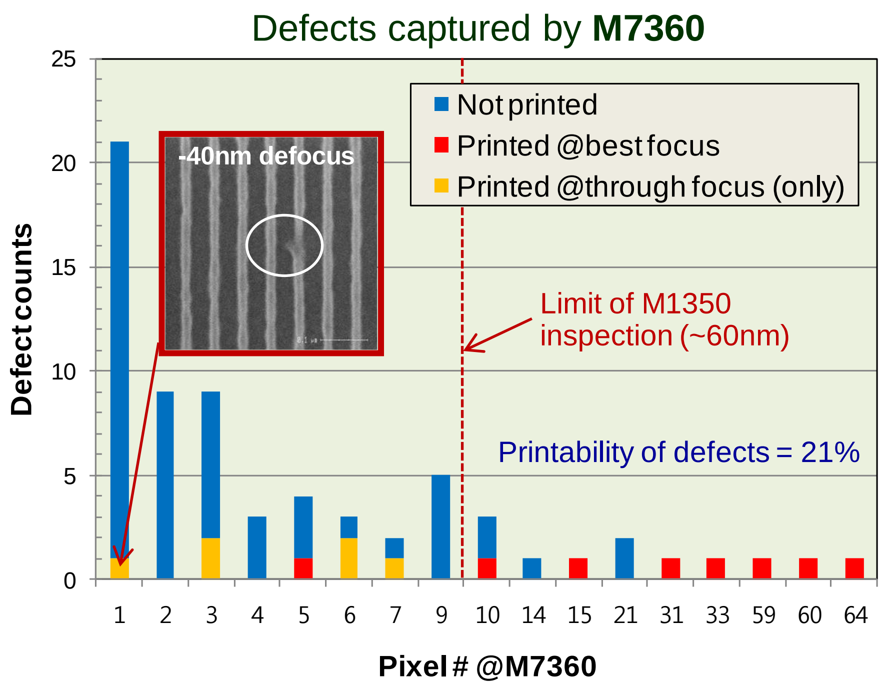
Detectability & printability of mask defects

	Blank defect	Mask inspection	SEM image	AFM on mask	Wafer image	Wafer inspection
Deep blank defect	Detected	Detected		 depth : ~ 50nm		Detected
Shallow blank defect	Not detected by M1350	Not detected		 size : 114.6, depth : 3.55nm		Detected
Pattern defect	-	Detected				Detected

- Shallow (small) blank defect is critical since it is hard to be detected in mask.
- Defect printability & inspectability depend on its size, shape, and location.

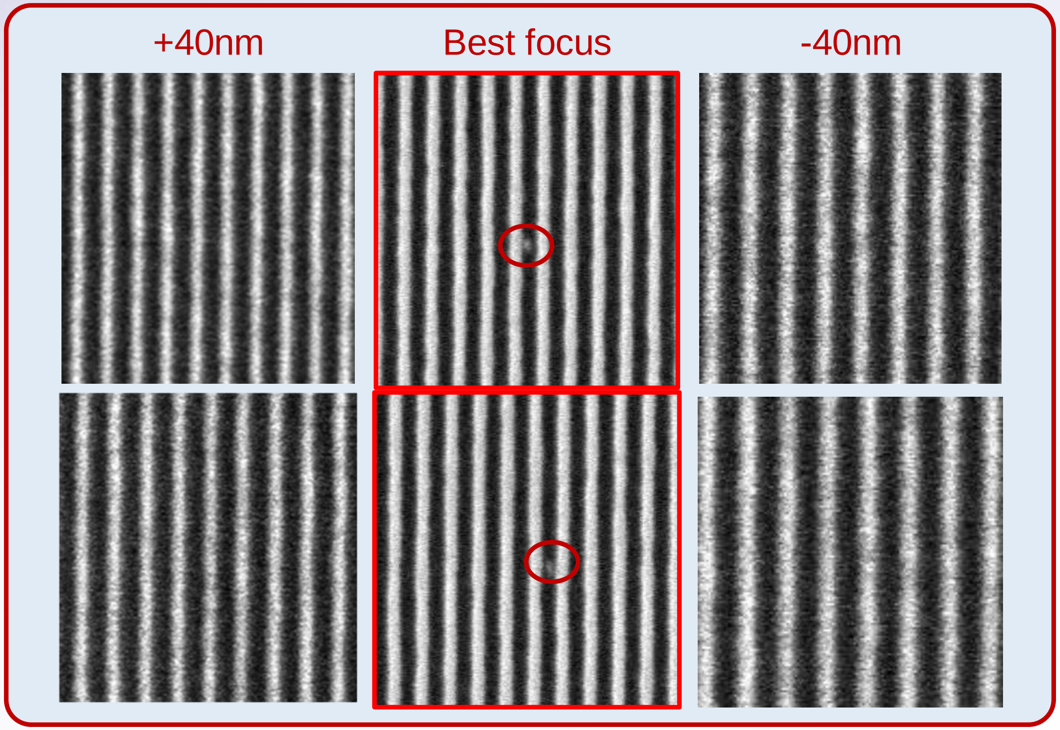
Wafer printability of real blank defects

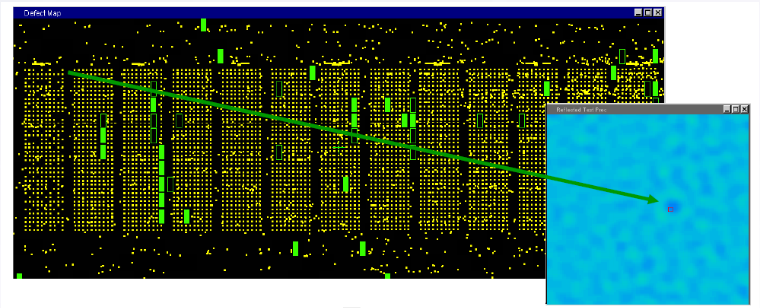




- Statistically, 20-30% of blank defects are printed on the patterned wafers at 32nm hp. But it depends on defect size as well as layout density.
- Even M7360, not to mention M1350, is not enough to catch all printable blank defects at 32nm hp node.

Wafer printability of real blank defects





Teron610 Phasur mode can catch blank defects with SEVD ~23nm and above sizes. (KLA-Tencor, SPIE 2011)

- More defects only detected by Teron610 Phasur mode are also printed on the wafer.
- These defects are only printed at best focus.
- Teron610 or equivalent blank inspection tool is required for 32nm hp node.

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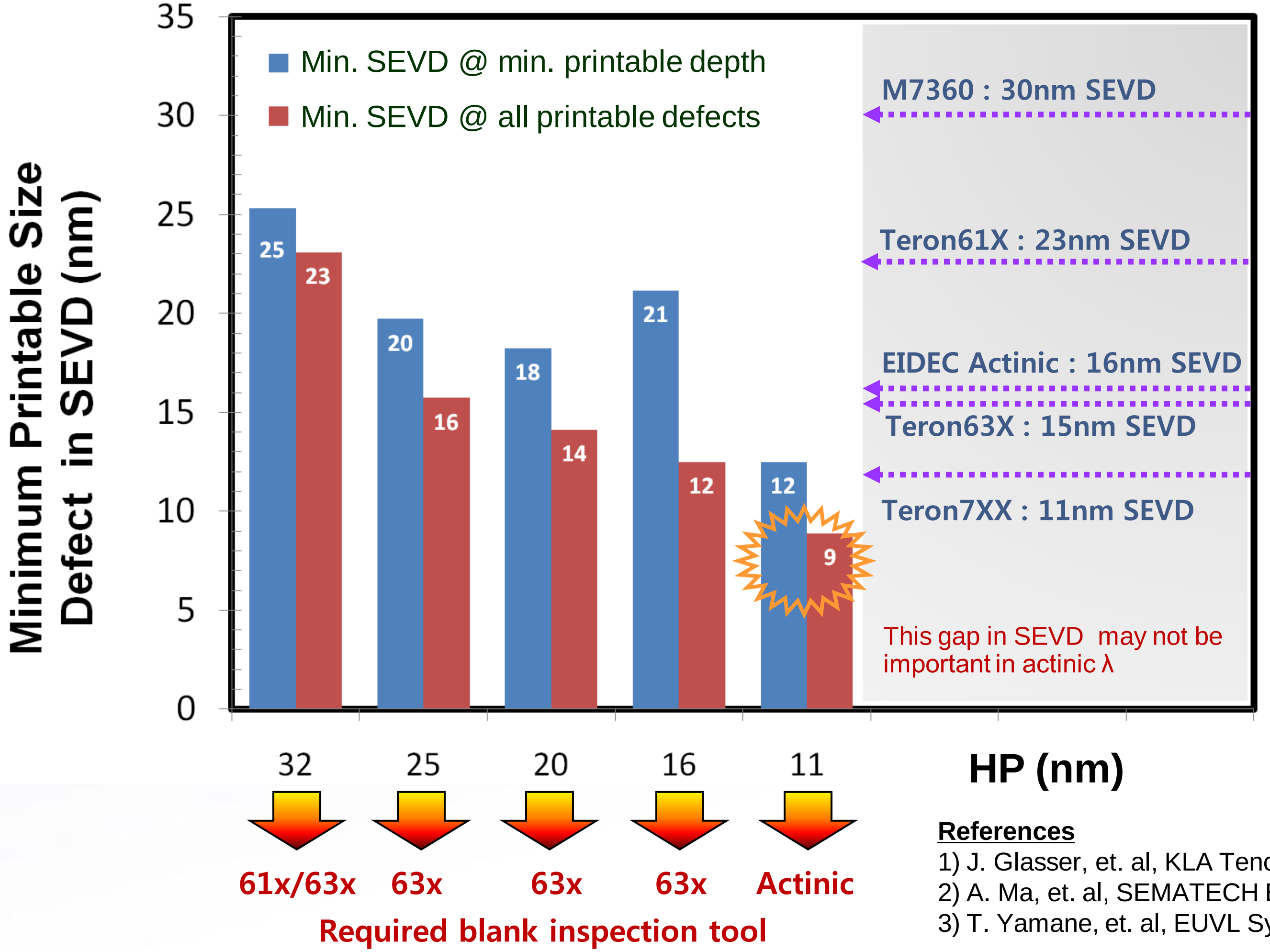
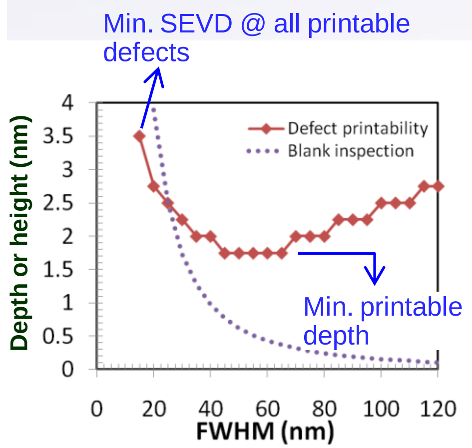
Phase defect printability simulations





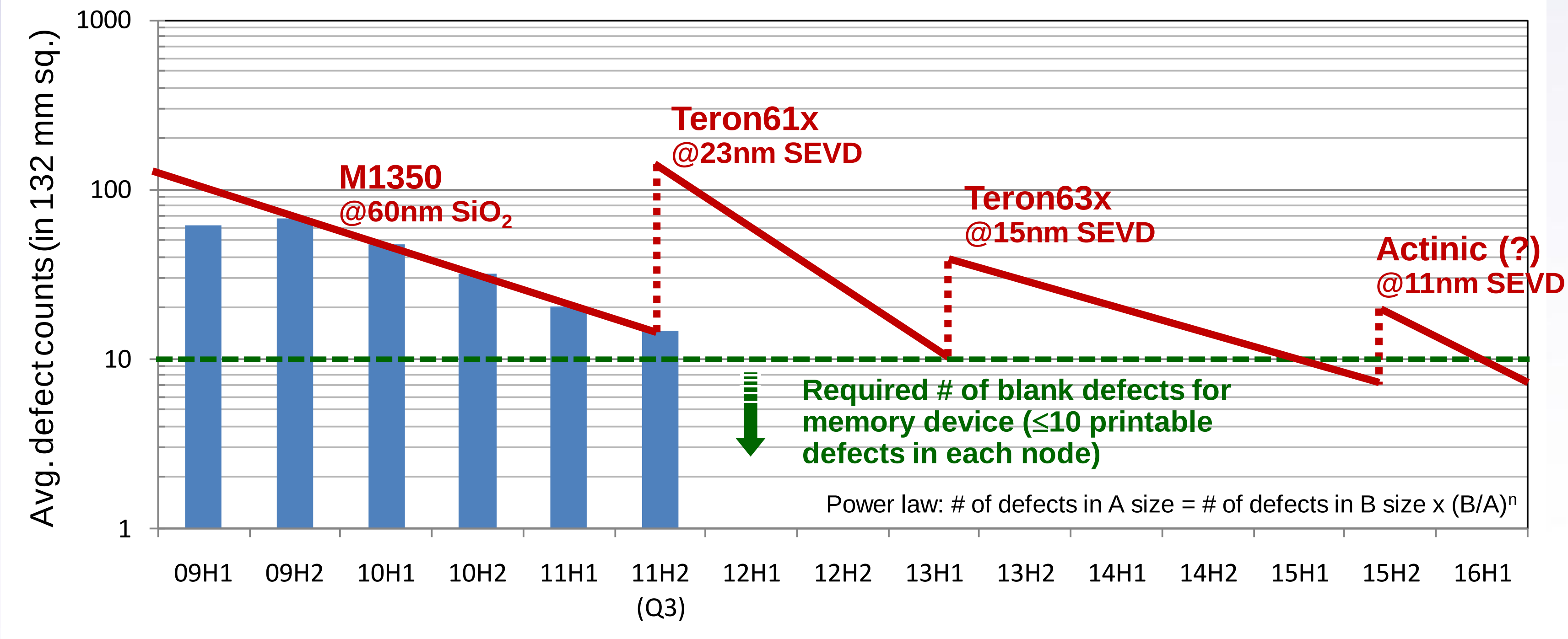
- 32nm HP: 0.33NA/Conv, Conv. abs.
- 25nm HP: 0.33NA/Ann, Conv. abs
- 20nm HP: 0.33NA/Quasar, Conv. abs
- 16nm HP: 0.33NA/Dipole, Conv. abs
- 11nm HP: 0.4xNA/Dipole, Conv. abs

References

1) J. Glasser, et. al, KLA Tencor, Proc. of SPIE Vol. Vol. 7748, 774808
2) A. Ma, et. al, SEMATECH EUVL Symposium, 2010
3) T. Yamane, et. al, EUVL Symposium, 2010

- BI tools and blanks to meet the requirements need to be prepared on time.

Roadmap for blank defect reduction



- Both blank suppliers achieved 1-digit number defects @ 60nm in size for champion blanks.
- ≤ 10 printable defects in each node are the requirements for HVM of memory device (blank defect compensation considered).
- For logic devices, tighter defect requirements should be applied.
- Corresponding BI tools and blanks in each node need to be developed on time for successful HVM of EUVL.

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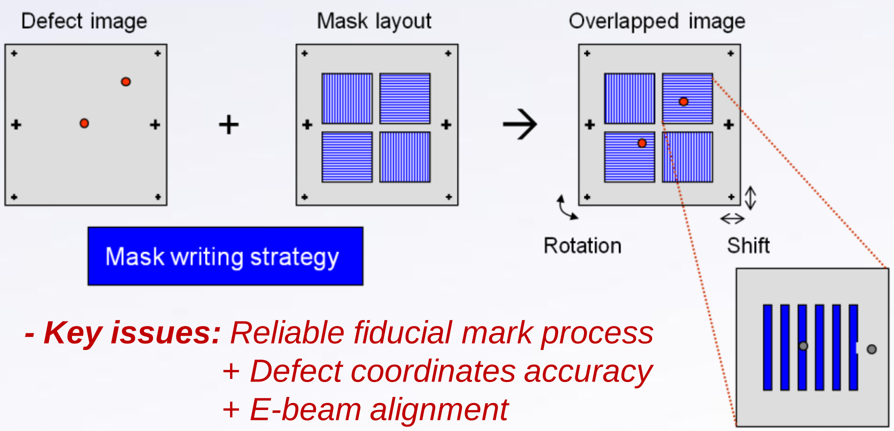
Additional defect mitigation process

- Additional defect mitigation technologies for “a few” blank defects should be developed when yield of defect free blank is low.

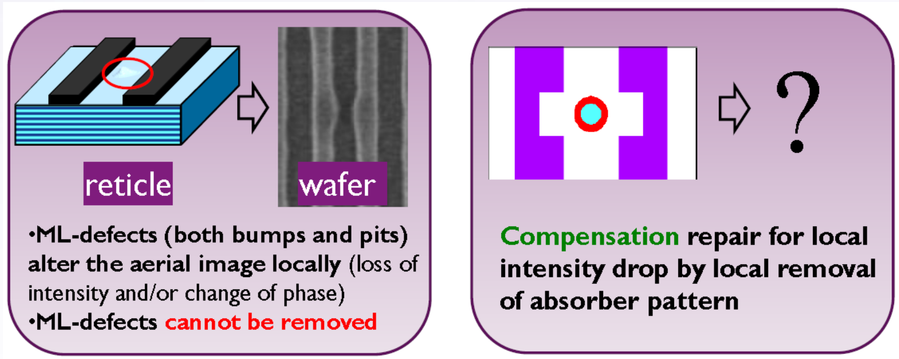
Fiducial mark & Defect compensation



***- Key issues:** Reliable fiducial mark process*
+ Defect coordinates accuracy
+ E-beam alignment

* SEMI standard meeting during SEMICON west (2009)

Phase defect repair



***- Key issues:** Defect review infra + Printing image estimation*

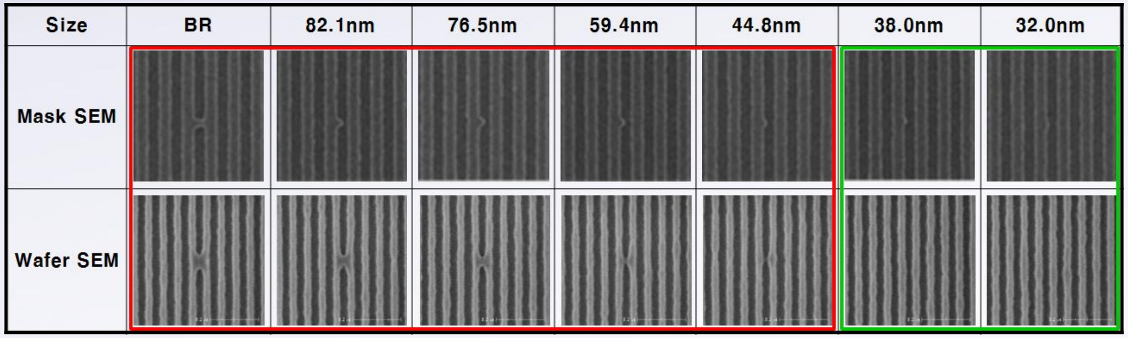
* Rik Jonckheere, Bacus presentation (2011)

Printable Phase defects → **Larger defects** → **Defect Compensation** → ***Memory & Logic***

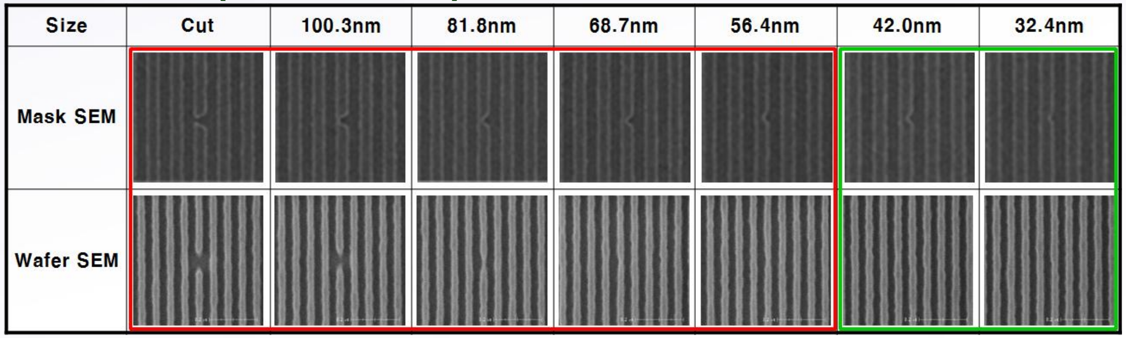
Printable Phase defects → **Smaller defects** → **Phase Defect Repair** → ***Logic (?)***

Pattern defect printability @30nm hp

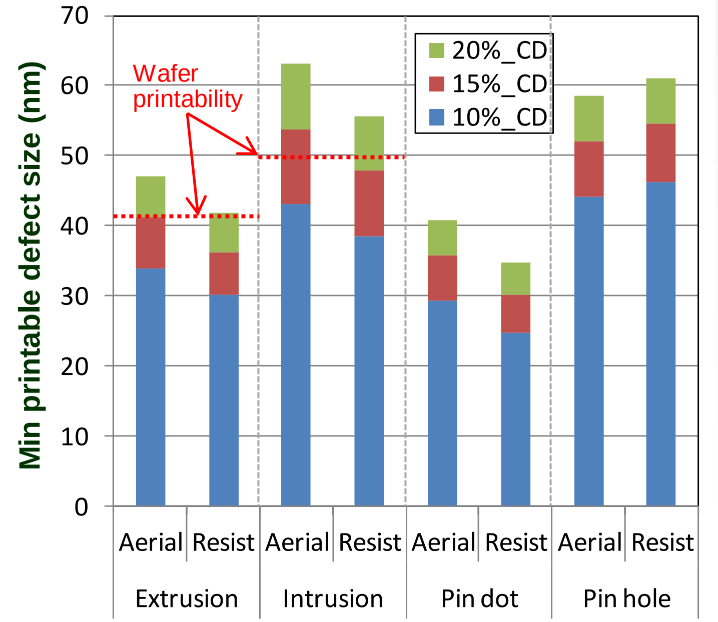
✓ Extrusion (Mask & Wafer)



✓ Intrusion (Mask & Wafer)



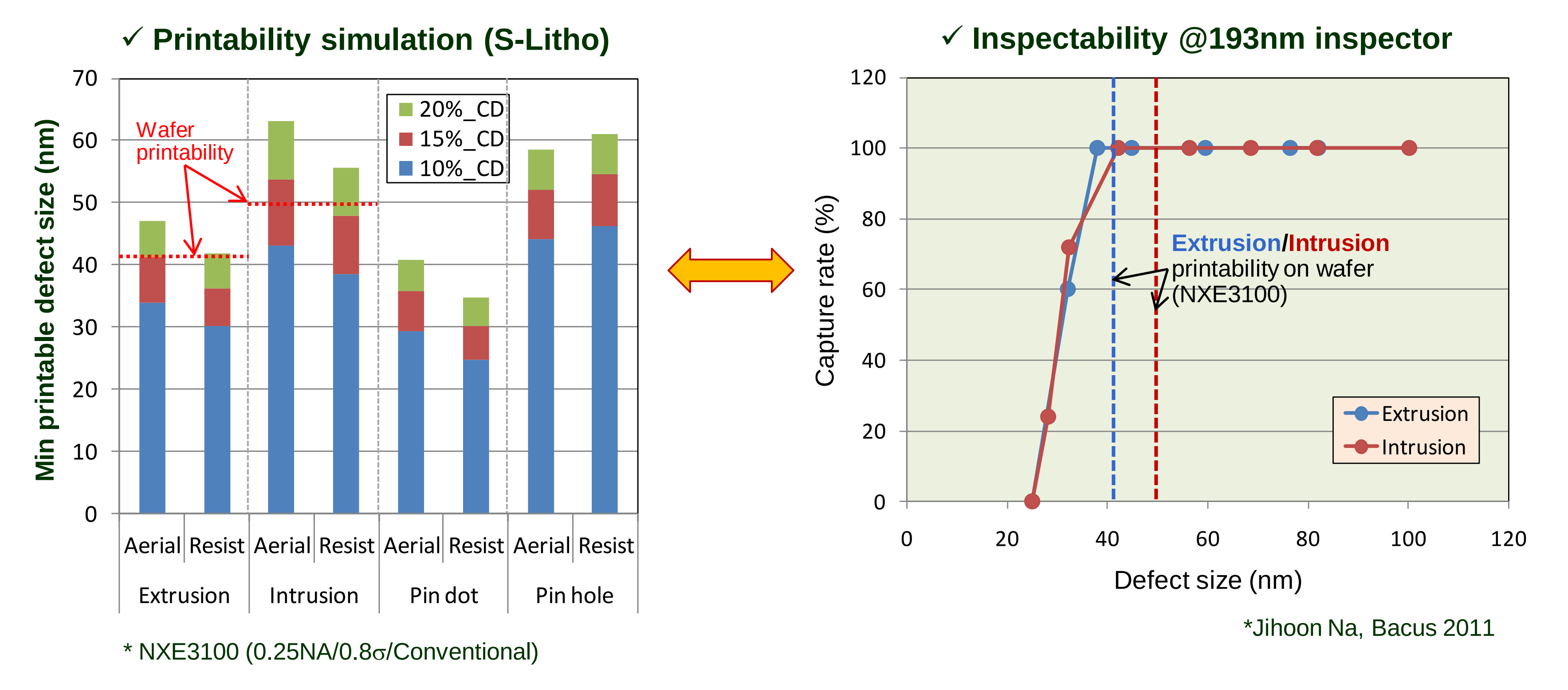
✓ Printability simulation (S-Litho)



* NXE3100 (0.25NA/0.8σ/Conventional)

- Defect sizes corresponding to15% CD variation in simulation are close to wafer printability results at 30nm hp.
- If LWR of wafer patterns is improved, minimum printable defect size might be decreased.

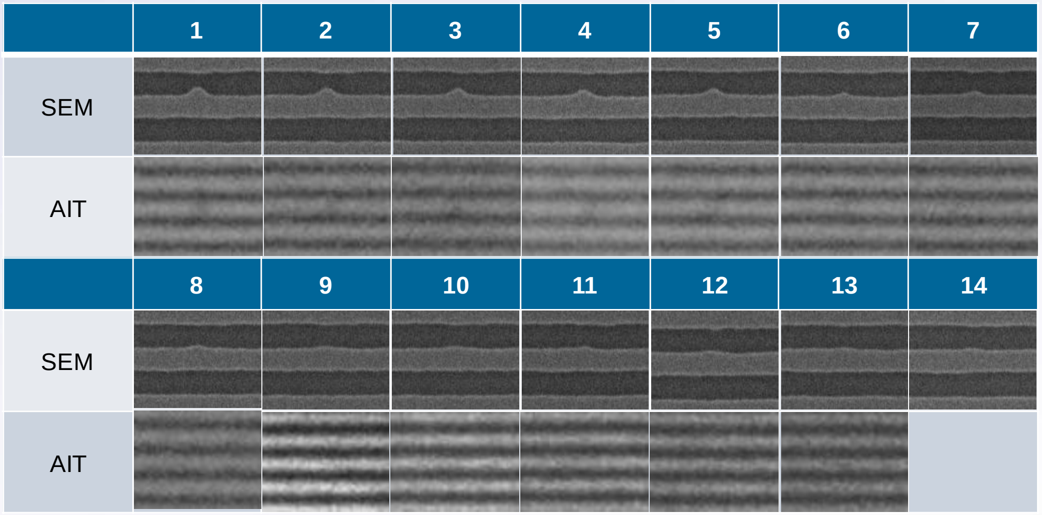
Printability & inspectability @30nm hp

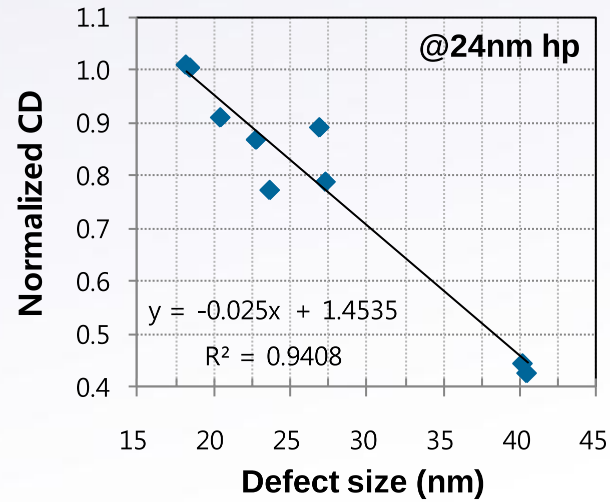


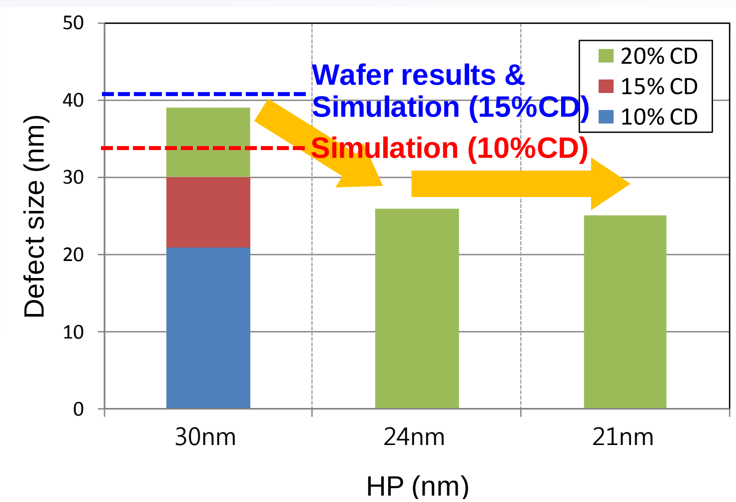
- Current 193nm mask inspection tool could meet requirements of defect sensitivity in 30nm hp node.
- How about next hp nodes?

Pattern defect printability estimation using AIT

Extrusion defect printability estimation by LBNL AIT (NA = 0.35)







- AIT can be used to evaluate defect printability below < 25nm hp since current EUVL scanner & resist performances are not enough.
- CD variations in AIT due to pattern defects are more sensitive than both litho simulation and wafer results.
- 20% CD variations in AIT is close to wafer results @30nm hp.

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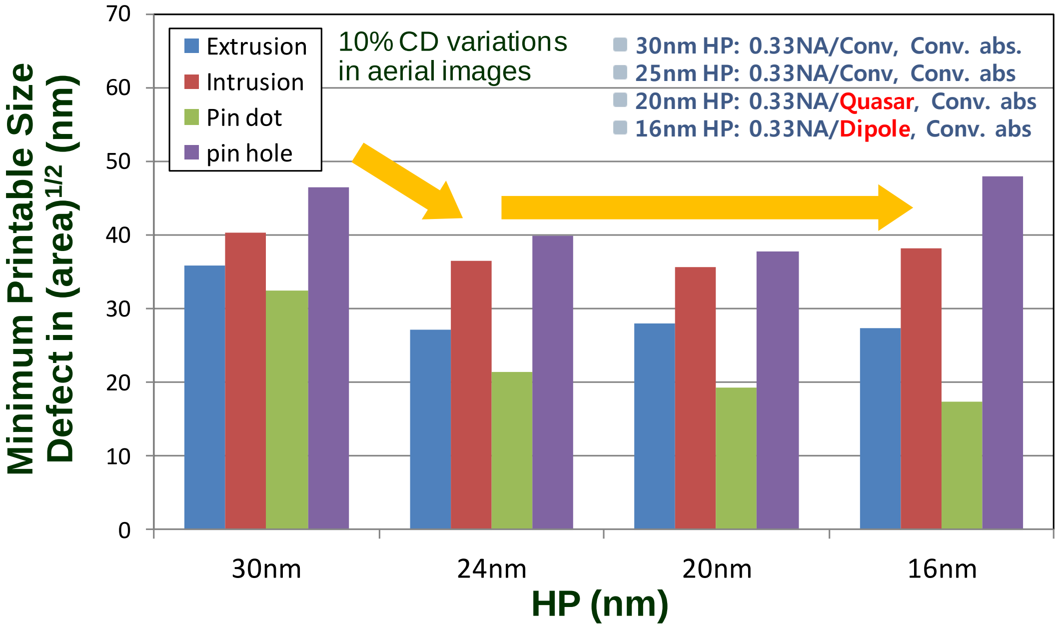
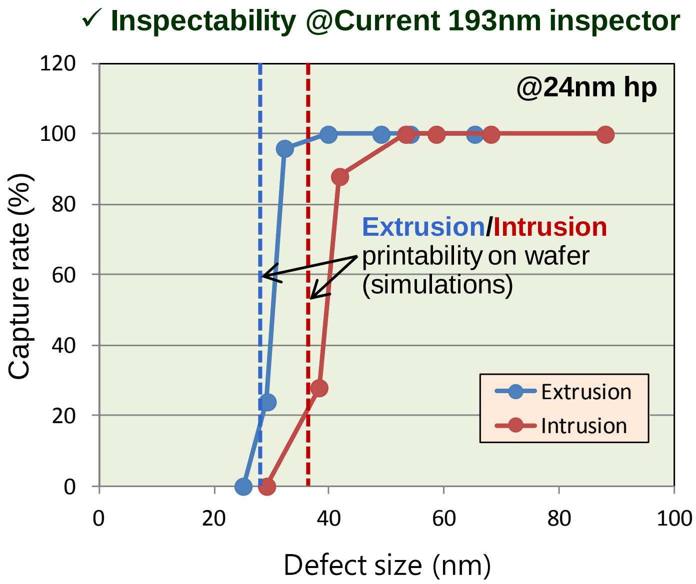
Pattern defect printability simulations

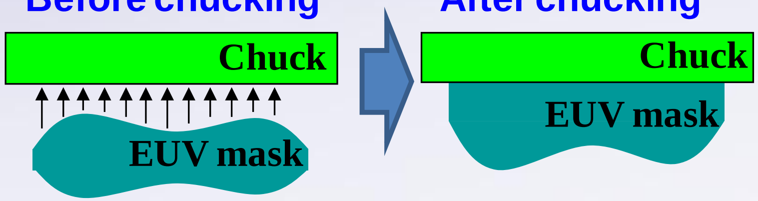


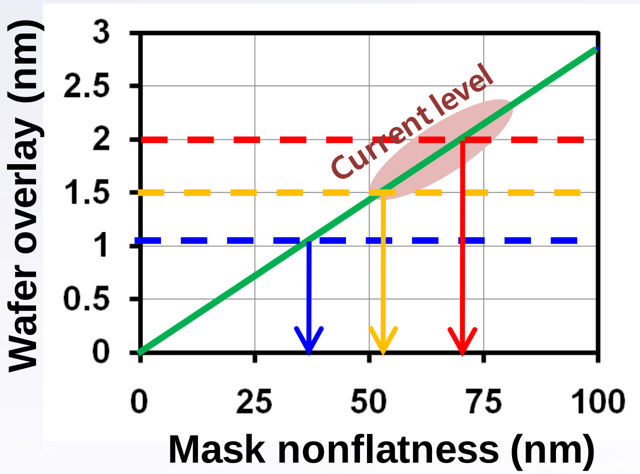


*Jihoon Na, Bacus 2011

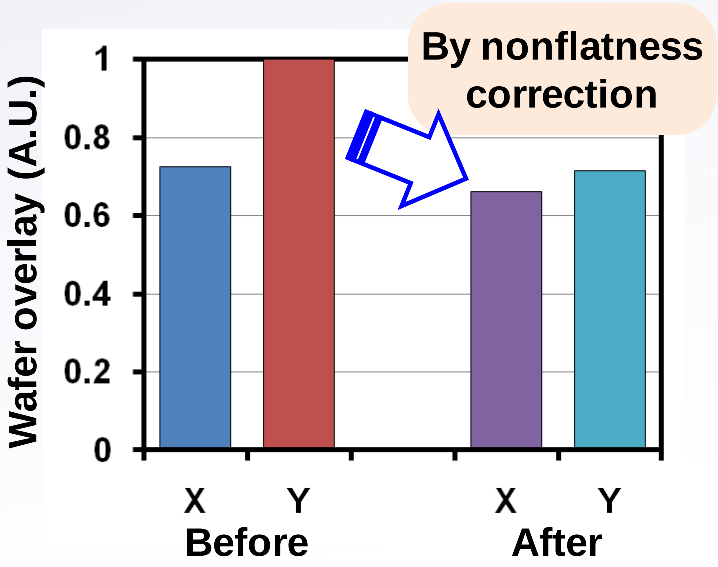
- Wafer printability of pattern defects strongly depends on illumination conditions in EUV scanner.
- Printable defect size decreases by 20-30% from 30 to 24nm hp and current PI tool is not enough for < 25nm applications. → Advanced PI tool & mask improvements to enhance defect sensitivity are required.
- Anyway, it seems that pattern defects are less sensitive than blank defects in wafer printability with decreasing hp node.

Non-flatness issues





Wafer writing test
on EUV nonflatness effect



- **Blank non-flatness and defects have trade-off relationships within a certain range.**
- **Wafer overlay due to EUV non-flatness effects**
  - Overlay specs, DCO & MMO, for NXE3100 are ≤4nm & ≤7nm, respectively.
  - 70nm non-flatness in EUVL mask results in 2nm wafer overlay error.
  - For 2x nm node device (<1nm overlay from flatness), EUV mask with 35nm flatness or equivalent non-flatness correction method should be developed.

Summary & conclusions

- **Requirements for EUVL mask blank in each hp node based on defect printability evaluation results are presented in this paper.**
- **Blank defects**
  - Both blank suppliers achieved 1-digit number defects @ 60nm (M1350) in blanks, but advanced BI tools to capture defects with ≤23nm in SEVD are required to catch all printable defects at 32nm hp node.
  - For memory devices, ≤10 printable blank defects in each node might be allowed for HVM. BI tools and blanks to meet the requirements need to be prepared on time.
  - Defect compensation and phase defect repair techniques should be developed to achieve defect-free masks using blanks with ≤10 printable defects.
- **Pattern defects**
  - Current 193nm PI tool in market could cover 30nm hp printability results but not enough for < 25nm applications.
  - Printable defect size decreases by > 20% from 30 to 24nm hp, so advanced PI tool and mask improvements to enhance defect sensitivity are required.
- **Non-flatness issues**
  - For 2x nm node device, EUV mask with 35nm flatness or equivalent non-flatness correction method should be developed.

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